26. (Amended) A method of forming a non-volatile electrically alterable semiconductor FLASH memory cell having a programming operation and an erase operation, with reduced, random, single bit data loss in a memory circuit comprising:

providing a silicon substrate;

fabricating a field oxide region and a channel region over or within the silicon substrate;

Growing an oxide over the channel region in an atmosphere enriched in Hydrogen isotope;

fabricating at least one gate member; and

passivating the memory cell having a programming operation and an erase operation, cmprising single bit data loss in an atmosphere that comprises Hydrogen isotope thereby reducing single bit data loss, wherein random single bit data loss is prevented in both the programming operation and the error operation.

37. (Amended) A method for overlaying source and drain regions of a non-volatile, electrically alterable semiconductor memory cell having a programming operation and an erase operation, with a thermal oxide layer thereby reducing random, single bit data loss in a memory circuit, comprising:

providing a silicon substrate and providing a memory cell, having a programming operation and an erase operation, the memory cell comprising single bit data;

defining source and drain regions in the silicon substrate; and

growing the thermal oxide layer over the source and drain regions in an atmosphere that comprises Hydrogen isotope thereby reducing single bit data loss in the programming operation and the erase operation in the memory cell.